REMARKS/ARGUMENT

The present Amendment is submitted for entry with an RCE. Claims 21-24, and 26-41 are pending after entry of this Amendment. Claims 21, 31, 36 and 41 are herein amended to positively recite that the low dielectric constant/carbon doped oxide layer is disposed directly over, and in direct contact with, the inorganic dielectric layer. Applicants further amend claims 21, 31, 36 and 41 to clarify the present invention by positively reciting that the low dielectric constant/carbon doped oxide layer defines a metallization line layer. Claim 41 is further amended to positively recite that the metallization lines are formed in a first portion of the second thickness of the low dielectric constant layer. Examiner is directed to page 13, line 20-page 15, line 6, page 10, line 21-page 11, line 5, page 12, lines 6-8, and Figures 2-7 for support of the claim amendments. No new matter is introduced.

Rejections under 35 U.S.C. §102

Claim 41 was rejected under 35 U.S.C. §102(e) as being anticipated by Parikh (U.S. Patent No. 6,225,207). Applicants respectfully traverse this rejection and request reconsideration.

In independent claim 41, as amended herein, Applicants claim a multi-layer dielectric disposed over a substrate for use in dual-damascene applications. The multi-layer dielectric includes a barrier layer disposed over the substrate, and an inorganic dielectric layer of a fluorine doped oxide disposed over the barrier layer. The inorganic dielectric layer has a first thickness. The multi-layer dielectric further includes a low dielectric constant layer of a carbon doped oxide disposed directly over, and in direct contact with, the inorganic dielectric layer. The low dielectric constant layer has a second thickness and defines a metallization line layer. Metallization lines are formed in a first portion of the second thickness of the low dielectric constant layer, and a via path is configured to be defined in an entire portion of the first thickness of the inorganic dielectric layer and in at least a portion of the second thickness of the low dielectric constant layer.

Parikh teaches methods for triple and quadruple damascene fabrication. According to the Parikh reference, triple damascene structures are fabricated in five consecutive "dielectric" layers. As is discussed in greater detail below, two of the five layers are in fact etch stop layers. The Parikh structures are fabricated using two etching sequences to form a power line trench, two

signal line trenches, and vias. The power line trench, signal line trenches, and vias are filled to form triple and quadruple damascene structures.

In order for a reference to anticipate a claim, each and every element as set forth in the claim must be found in the reference, either expressly or inherently described. MPEP 2131. Applicants respectfully submit that the patent to Parikh fails to teach each and every element of Applicants' independent claim 21. Specifically, Parikh fails, at least, to teach a barrier layer disposed over the substrate, fails to teach a low dielectric constant layer having a second thickness and defining a metallization layer, and fails to teach metallization lines formed in a first portion of the second thickness of the low dielectric constant layer, and a via path configured to be defined in an entire portion of the first thickness of the inorganic dielectric layer and in at least a portion of the second thickness of the low dielectric constant layer.

The structure disclosed by Parikh does not teach the claimed structure of Applicants' independent claim 41. The Office has asserted that layer 312 of the Parikh is a barrier. According to col. 6, lines 61-62, layer 312 is characterized as a "first dielectric layer." At col. 9, lines 2-5, layer 312 is a low k dielectric.

The Office has further asserted that layer 316 is a low dielectric constant layer. Applicants have further amended independent claim 41 to specifically recite that the low dielectric constant layer defines a metallization line layer. While the bottom of power line trench 325 is in third dielectric layer 316, only a portion of a metallization line in a lower part of power line is in third dielectric layer 316. Parikh's third dielectric layer 316 does not define a metallization line layer. In other words, power line 325 extends into, and terminates in, third dielectric layer 316, but third dielectric layer 316 does not define a metallization line layer.

Parikh does not disclose metallization lines being formed in a first portion of the second thickness of the low dielectric constant layer, and a via path defined in an entire portion of the first thickness of the inorganic dielectric layer and in at least a portion of the second thickness of the low dielectric constant layer. In the Parikh reference (Figure 3E), a metallization line 325 is defined in and through all of layers 316, 318, and 320. Layer 318 is an etch stop layer.

For at least the above reasons, the Parikh reference fails to teach each and every element as set forth in Applicants' independent claim 41. Applicants therefore respectfully request the rejection under 35 U.S.C. §102 be withdrawn.

Rejections under 35 U.S.C. §103

Claim 21 was rejected under 35 U.S.C. §103(a) as being unpatentable over Parikh in view of Yu et al. (U.S. Patent No. 6,187,663). This rejection is traversed, and Applicants request reconsideration in view of claim amendments and the following argument.

The present invention, as described and illustrated by Applicants, and subsequently claimed in independent claim 21 as amended herein, claims a multi-layer dielectric layer over a substrate for use in dual-damascene applications. The multi-layer dielectric layer includes a barrier layer disposed over the substrate, an inorganic dielectric layer having a dielectric constant of about 4 disposed over the barrier layer, and a low dielectric constant layer disposed directly over the inorganic dielectric layer. The low dielectric constant layer is configured to receive metallization line trenches and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references when combined must teach or suggest all the claim limitations. (MPEP §2143). Applicants respectfully submit the Office has failed to establish a prima facie case of obviousness.

The patent to Parikh is described above. Yu et al. teach a method for fabricating a copper damascene structure which includes two composite low-k dielectric layers each fabricated of two layers of low-k materials, and the two composite layers are separated by an etch stop layer of silicon oxynitride.

The Office asserts that Parikh teaches layer 312 of Figure 3E is a barrier layer. As described above, Parikh teaches layer 312 is a first dielectric layer, and that first dielectric layer 312 is a low k dielectric.

The Office asserts that Parikh teaches that layer 314 is an inorganic dielectric layer disposed over the barrier layer 312. As described above, layer 312 is described as a first dielectric layer, and that layer 312 is a low k dielectric layer. Layer 314 is an etch stop layer. See col. 7, lines 9-11: "Dielectric layers 314 and 318 are etch stop layers having similar etching

characteristics." While etch stop layer 314 may in fact be an inorganic dielectric (col. 8, line 76-col. 9, line 2), etch stop layer 314 is not disposed over a barrier layer in the Parikh reference.

Applicants have amended claim 21 to specifically recite that the low dielectric constant layer is configured to receive metallization line trenches to define a metallization line layer, and the inorganic dielectric layer is configured to receive vias during a dual-damascene process. Parikh does not teach a dual-damascene process. The low dielectric constant layer, as identified by the Office to be layer 316, does not define a metallization line layer. As described above, the bottom of power line trench 325 is in third dielectric layer 316, and only a portion of the metallization line, a lower part of power line 325, is in third dielectric layer 316. Parikh's third dielectric layer 316 does not define a metallization line layer. In other words, power line 325 extends into, and terminates in, third dielectric layer 316, but third dielectric layer 316 does not define a metallization line layer.

The Office further asserts that Parikh is silent about the inorganic dielectric layer having a dielectric constant of about 4. The Office then asserts that the k value is considered to involve routine optimization and within the level of ordinary skill in the art. Applicants respectfully disagree. While the Office has asserted that the k value of the dielectric material is one of routine optimization, the Office has overlooked that a k value of a dielectric material is of material importance to the formation of a semiconductor device or structure, and to the resulting structure so formed, which is well known in the art. The k value of a dielectric is not merely a parameter of, for example, temperature or concentration, and as is well known in the art, the selection of a low k dielectric or election not to use a low k dielectric defines and determines the material properties and function of the resulting structure or device. Applicants have specifically claimed a k value of the inorganic dielectric layer of about 4 to specifically claim that the inorganic dielectric layer is ***not*** a low k dielectric layer. The Office then cites the combination of Yu et al. to capture the dielectric constant of about 4, although using the value in Yu et al. of 3.5-3.7 as close enough.

Applicants respectfully disagree with the Office's characterization. However, even if the combination with Yu et al. were to capture what the Office needed to find in a dielectric constant value, the combination does not sufficiently revive the Parikh reference to teach or suggest all the claim limitations.

For at least the above reasons, Applicants submit that either Parikh alone, or the combination of Parikh with Yu et al. fail to teach or suggest all the claim limitations, and therefore do not render Applicants' independent claim 21 obvious. Applicants respectfully request that the 35 U.S.C. §103 rejection of claim 21 be withdrawn. The fact that all of Applicants' claim limitations are not found in the asserted combination establishes that the Office has failed to present a *prima facie* case of obviousness, and is not intended to address further issues, for example, of whether or not any motivation exists to assert such a combination.

Claims 21-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wang et al. (U.S. Patent No. 6,255,735) in view of Yu et al. The rejection is traversed, and Applicants request reconsideration in view of claim amendments and submitted argument.

Wang et al. disclose a conductive layer (10) over which an etch stop layer (12) has been formed. A first dielectric layer (14) is formed over the etch stop layer (12), and a second dielectric layer (18) is formed over the first dielectric layer (14). The second dielectric layer (18) is a low k dielectric material that is spin-coated on the first dielectric layer (14). Wang et al. describe the first dielectric layer (14) as formed of a low k dielectric material with a k value of less than 4 (see col. 5, lines 32-35), and the second dielectric layer (18) also being comprised of a low k dielectric material (col. 5, lines 55). The second low k dielectric material is disclosed to require a different sensitivity than the low k dielectric material in the first dielectric layer (14) to at least one etchant chemistry (col. 5, lines 60-63), although it is not disclosed that one or the other layer needs to have the lower of the two low k values.

Wang et al., do not disclose an inorganic dielectric layer disposed over a barrier, the inorganic dielectric layer having a dielectric constant of about 4, and a low dielectric constant layer disposed directly over and in direct contact with the inorganic dielectric layer.

The Office asserts that Wang et al. is silent about the inorganic dielectric layer having a dielectric constant of about 4. Applicants respectfully disagree. Wang et al. explicitly teach a low k dielectric over a low k dielectric (see, for example, the Abstract, col. 5, lines 7-11, col. 6, lines 1-11, col. 8, lines 12-17, etc.). Applicants have specifically recited a k value of about 4 to specifically claim an inorganic dielectric layer that is not a low k dielectric layer.

The Office then asserts that the k value is considered to involve routine optimization and within the level of ordinary skill in the art. Applicants respectfully disagree. While the Office has asserted that the k value of the dielectric material is one of routine optimization, the Office has overlooked that a k value of a dielectric material is of material importance to the formation of a semiconductor device or structure, and to the resulting structure so formed, which is well known in the art. The k value of a dielectric is not merely a parameter of, for example, temperature or concentration, and as is well known in the art, the selection of a low k dielectric or election not to use a low k dielectric defines and determines the material properties and function of the resulting structure or device. Applicants have specifically claimed a k value of the inorganic dielectric layer of about 4 to specifically claim that the inorganic dielectric layer is ***not*** a low k dielectric layer. The Office then cites the combination of Yu et al. to capture the dielectric constant of about 4, although the Office characterizes the k value in Yu et al. of 3.5-3.7 as close enough.

Applicants respectfully submit that the 3.5-3.7 k value taught by Yu et al. is not close enough. Moreover, Wang et al. teach low k over low k. There simply isn't any motivation to change the entire premise of the Wang et al. structure to have non-low k over low k.

For at least the above reasons, Applicants submit that the combination of Wang et al. and Yu et al. do not render obvious Applicants' independent claim 21. Dependent claims 22-23, depending directly or indirectly from independent claim 21 are therefore also not rendered obvious. Applicants request the §103 rejection be withdrawn.

Claims 24 and 26-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wang et al. in view of Yu et al. as applied to claim 23, and further in view of Usami (U.S. Patent No. 6,077,574). Applicants traverse this rejection and request reconsideration.

For at least the reasons stated above, Applicants submit the combination of Wang et al. with Yu et al. do not render Applicants' claim 23 obvious. Usami teaches a process for forming a plasma CVD fluorine-doped SiO_2 dielectric film in which a feed gas is supplied to a plasma CVD apparatus. The feed gas includes, among various gases, carbon and fluorine gases which are controlled independently of each other resulting in a silicon-based SiO_2 dielectric film doped with fluorine and carbon for a low dielectric constant value.

Whether or not Usami captures additional features that the asserted combination of Wang et al. with Yu et al. also do not teach, the additional features do not salvage the failure of the combination of Wang et al. with Yu et al. to render Applicants' independent claim 21, and therefore dependent claim 23, obvious. Applicants therefore request the rejection of claims 24 and 26-30 under 35 U.S.C. §103(a) as being unpatentable over Wang et al. in view of Yu et al. as applied to claim 23, and further in view of Usami be withdrawn.

Claims 31-40 were rejected under 35 U.S.C. §103(a) as being unpatentable over Smith (U.S. Patent No. 6,277,733) in view of Usami. Applicants traverse this rejection and request reconsideration.

In independent claim 31, as amended herein, Applicants claim a multi-layer inter-metal dielectric semiconductor structure. The multi-layer inter-metal dielectric semiconductor structure includes a barrier layer disposed over a base dielectric layer, and an inorganic dielectric layer of an un-doped TEOS oxide disposed over the barrier layer. The multi-layer inter-metal dielectric semiconductor structure further includes a low dielectric constant layer of a carbon doped oxide disposed directly over, and in direct contact with, the inorganic dielectric layer. The low dielectric constant layer is configured to receive metallization line trenches to define a metallization line layer, and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

In independent claim 36, as amended herein, Applicants claim a dielectric structure for dual-damascene applications. the dielectric structure includes a barrier disposed over a base dielectric, an inorganic dielectric layer of a fluorine doped oxide disposed over the barrier, and a low dielectric constant layer of a carbon doped oxide disposed directly over, and in direct contact with, the inorganic dielectric layer. The low dielectric constant layer is configured to receive metallization line trenches to define a metallization line layer, and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

Smith teaches a barrier (422) over a conductor (420). A low dielectric constant layer (424) is formed over the barrier (422), and a hardmask (426) is formed over the low dielectric constant layer (424). Another low dielectric constant layer (430) is formed over the hardmask (426). While the hardmask (426) may be etched for via formation, when the vias are formed, the low dielectric

constant layer (430) over the etched portion is removed (Fig. 2d). Therefore, Smith teaches a low dielectric constant layer over a hardmask over a low dielectric constant layer over a barrier over a substrate. Smith does not teach or suggest a low dielectric constant layer disposed directly over, and in direct contact with, an inorganic dielectric layer.

Applicants have amended independent claim 31 and 36 to positively recite that the low dielectric constant layer of carbon doped oxide is disposed directly over and in direct contact with the inorganic dielectric layer. The Office asserts that even if Applicants' were to recite "directly in contact with," Smith teaches directly in contact with in Figure 2c. Applicants respectfully disagree, and request the Office re-consider the assertion. Figure 2c, as is described more fully below, does not teach or suggest a low dielectric constant layer disposed directly over, and in direct contact with, an in inorganic dielectric layer.

As illustrated in Figure 2h, the patent to Smith teaches a low dielectric constant layer 430 over a hardmask 426 over a low dielectric constant layer 424 over a barrier 422 over a substrate 416 (generally, or the combination of 414 and 416, having conductor 420 formed therein). The Office asserts the combination of Smith and Usami, as the patent to Smith fails to teach a low dielectric constant layer of carbon doped oxide. Applicants respectfully submit that whether or not the patent to Usami captures the feature of using carbon doped oxide, the asserted combination still fails to teach or suggest all of Applicants' claim limitations as recited in independent claims 31 and 36. Neither Smith nor Usami teach a low dielectric constant layer disposed directly over, and in direct contact with, an inorganic dielectric layer. The Office has suggested that Figure 2c of Smith teaches a low dielectric constant layer 430 disposed directly over, and in direct contact with, an inorganic dielectric layer 424. Applicants respectfully point out that the Office has identified a figure showing a process step in the formation of the structure of Smith. As described at col. 3, lines 56-57, Figure 2c corresponds to process step 306 of Figure 1, dielectric deposition. As is well known in the art, deposition of a dielectric, or other material, in one phase of fabrication is typically followed by etch, CMP, or other such process step to then define a pattern or feature and then the removal of the deposited material for feature formation. The Office is suggesting that Figure 2c, which is not a completed structure, might teach or suggest Applicants' claimed complete structure. If this were true, then countless figures in countless references showing structures in the process of formation would invalidate countless legitimate, novel inventions. That Figure 2c of

Smith shows that, at one point in the formation of the ultimate structure, a low dielectric constant dielectric is deposited over the hardmask having a feature defined therein, and therefore the deposited material is deposited into the feature during that process step, ***does not*** teach or suggest the ultimate structure. In the Smith reference, the ultimate feature has the low k dielectric completely removed from within the feature, which is typical of the structure being described. That the low k dielectric was initially deposited over the layers during fabrication, however, does not teach or suggest what the ultimate structure, design, or function of that circuit or structure will be.

For at least the above reasons, Applicants submit that the combination of Smith and Usami do not teach or suggest all of Applicants claim limitations as recited in independent claims 31 and 36. Claims 31 and 36 are therefore submitted to be patentable under 35 U.S.C. §103(a) over Smith in view of Usami. Further, dependent claims 32-35 and 37-40, depending directly or indirectly from one of independent claims 31 and 36, are likewise patentable. Applicants respectfully request the §103 rejections be withdrawn.

In view of the foregoing, Applicants respectfully request reconsideration of claims 21-24 and 26-41. Applicants submit that all claims are in condition for allowance. Accordingly, a notice of allowance is respectfully requested. If Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6905. If any additional fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM1P106D). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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